SEMICONDUCTOR FILMS ON FLEXIBLE IRIDIUM SUBSTRATES

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[0001]. The United States Government has rights in this invention pursuant to contract no. DE-AC05-00OR22725 between the United States Department of Energy and UT-Battelle, LLC.

[0002]. FIELD OF THE INVENTION

[0003]. The present invention relates to semiconductor films, and more particularly to biaxially textured semiconductor films and flexible Ir-based support substrates therefor.

[0004]. BACKGROUND OF THE INVENTION

[0005]. Various electromagnetically useful materials have been applied epitaxially to biaxially textured support materials. An important class of substrates is known as rolling assisted, biaxially textured substrates (RABiTS). Biaxial texture in a substrate refers to situation when all the grains in a polycrystalline substrate are aligned within a certain angular range with respect to one another. A polycrystalline material having biaxial texture of sufficient quality for electromagnetic applications can be generally defined as being characterized by an x-ray diffraction phi scan peak of no more than 20° full-width-half-maximum (FWHM) and a omega-scan of 10° FWHM.. The X-ray phi-scan and omega-scan measure the degree of in-plane and out-of-plane texture respectively. An example of biaxial texture is the cube texture with orientation {100}<100>, wherein the (100) crystallographic plane of all grains is parallel to the substrate surface and the [100] crystallographic direction is aligned along the substrate length. Other suitable definitions have also been set forth in varying terms.

[0006]. It is helpful to review some of the prior work that the present invention builds upon. The entire disclosure of each of the following U.S. patents is incorporated herein by reference:

[0007]. U.S. Patent No. 5,739,086 issued on April 14, 1998 to Goyal, et al.

[0008]. U.S. Patent No. 5,964,966 issued on October 12, 1999 to Goyal, et al.

[0009]. U.S. Patent No. 5,968,877 issued on October 19, 1999 to Budai, et al.

[0010]. U.S. Patent No. 5,972,847 issued on October 26, 1999 to Feenstra, et al.

[0011]. U.S. Patent No. 6,077,344 issued on June 20, 2000 to Shoup, et al.

[0012]. U.S. Patent No. 6,114,287 issued on September 5, 2000 to Lee, et al.

[0013]. U.S. Patent No. 6,150,034 issued on November 21, 2000 to Paranthaman, et al.

[0014]. U.S. Patent No. 6,159,610 issued on December 12, 2000 to Paranthaman, et al.

[0015]. U.S. Patent No. 6,180,570 issued on January 30, 2001 to Goyal.

[0016]. U.S. Patent No. 6,256,521 issued on July 3, 2001 to Lee, et al.

[0017]. U.S. Patent No. 6,261,704 issued on July 17, 2001 to Paranthaman, et al.

[0018]. U.S. Patent No. 6,270,908 issued on August 7, 2001 to Williams, et al.

[0019]. U.S. Patent No. 6,331,199 issued on December 18, 2001 to Goyal, et al.

[0020]. U.S. Patent No. 6,440,211 issued on August 27, 2002 to Beach, et al.

[0021]. U.S. Patent No. 6,447,714 issued on September 10, 2002 to Goyal, et al.

[0022]. U.S. Patent No. 6,451,450 issued on September 17, 2002 to Goyal, et al.

[0023]. U.S. Patent No. 6,617,283 issued on September 9, 2003 to Paranthaman, et al.

[0024]. U.S. Patent No. 6,645,313 issued on November 11, 2003 to Goyal, et al.

[0025]. U.S. Patent No. 6,670,308 issued on December 30, 2003 to Goyal.

[0026]. U.S. Patent Application Publication No. 20030143438 published on July 31, 2003 to Norton, et al.

[0027]. U.S. Patent Application Serial No. 10/324,883 filed on December 19, 2002.

[0028]. U.S. Patent Application Serial No. 10/620,251 filed on July 14, 2003.

[0029]. U.S. Patent No. 6,632,539 issued on October 19, 2003 to Iijima et al.

[0030]. U.S. Patent No. 6,214,772 issued on April, 10, 2001 to Iijima et al.

[0031]. U.S. Patent No. 5,650,378 issued on July, 22, 1997 to Iijima et al.

[0032]. U.S. Patent No. 5,872,080 issued on February 19, 1999 to Arendt et al.

[0033]. U.S. Patent No. 6,190,752 issued on February 20, 2001 to Do et al.

[0034]. U.S. Patent No. 6,265,353 issued on July 24, 2001 to Kinder et al.

[0035]. U.S. Patent No. 5,432,151 issued on July 11, 1995 to Russo et al.

[0036]. U.S. Patent No. 6,361,598 issued on March 26, 2002 to Iijima et al.

[0037]. Moreover, there are other known routes to fabrication of biaxially textured, flexible electromagnetic devices known as ion-beam-assisted deposition (IBAD) and inclined-substrate deposition (ISD). IBAD processes are described in U.S. Patents Nos. 6,632,539, 6,214,772, 5,650,378, 5,872,080, 5,432,151 and 6,361,598; ISD processes are described in U.S. Patents Nos. 6,190,752 and 6,265,353; all these

patents are incorporated herein by reference. In the IBAD and ISD processes a flexible, polycrystalline, untextured substrate is used and then a biaxially textured layer is deposited on this substrate.

[0038]. Semiconductor research and development efforts are often focused on increasing the speed of electronic devices. Ultimately, there are only two ways to increase the speed of transistor switches based on existing semiconductor technologies. The first is to reduce the size of the structures on the semiconductor, thereby obtaining smaller transistors that are closer together and use less power. The second is to use alternative semiconductor materials that inherently switch faster. For example, the band-gap effects associated with GaAs's 3:5 valance structure mean that these transistors switch approximately eight times faster and use one-tenth the power of their silicon counterparts. Use of SiC, cubic boron nitride (cBN) and diamond based devices would potentially even faster. Hence, successful fabrication of semiconductors other than Si using industrially scalable routes if of great interest.

[0039]. It has recently been demonstrated that epitaxy of diamond films can be obtained on Ir surfaces. M. Schreck et al. have shown that single-crystal Ir films can be deposited by electron beam evaporation on rigid, single crystal $SrTiO_3$ surfaces. However, such a process is limited to substrate selections available – rigid single crystal ceramic substrates such as $SrTiO_3$. Such a process cannot be used to make continuous long lengths or wide area devices since it is limited to the size in which SrTiO3 single crystals can be fabricated. Moreover, SrTiO3 are not flexible. Flexible refers to the ability of the substrate to be bent slightly withour cracking.

[0040]. OBJECTS OF THE INVENTION

[0041]. Accordingly, objects of the present invention include the provision of biaxially textured semiconductor materials, especially diamond, and flexible support materials therefor. Further and other objects of the present invention will become apparent from the description contained herein.

[0042]. SUMMARY OF THE INVENTION

[0043]. In accordance with one aspect of the present invention, the foregoing and other objects are achieved by a laminated semiconductor article that includes a flexible substrate; a biaxially textured Ir-based buffer layer over the flexible substrate; and at least one epitaxial layer of a semiconductor over the Ir buffer layer.

[0044]. In accordance with another aspect of the present invention, a laminated semiconductor article including a flexible substrate; a biaxially textured buffer system on the flexible substrate; an epitaxial Ir-based buffer layer on the buffer system; and at least one epitaxial layer of a semiconductor over the Ir buffer layer.

[0045]. In accordance with a further aspect of the present invention, a laminated semiconductor article including a flexible Ir-based substrate; and at least one epitaxial layer of a semiconductor over the flexible Ir substrate.

[0046]. BRIEF DESCRIPTION OF THE DRAWINGS

[0047]. Figs. 1-6 are schematic illustrations of various buffer layer architectures in accordance with the present invention.

[0048]. For a better understanding of the present invention, together with other and further objects, advantages and capabilities thereof, reference is made to the following disclosure and appended claims in connection with the above-described drawings.

[0049]. DETAILED DESCRIPTION OF THE INVENTION

[0050]. The invention provides methods for the fabrication of sharply biaxially textured substrates of various materials and semiconductor films epitaxially deposited thereon. As used herein, the phrase "sharply biaxially textured" is defined herein to mean a texture that approaches the texture provided by a bulk single crystal. A bulk article which is sharply biaxially textured has a crystallographic orientation such that all the grains in the substrate are crystallographically aligned within 7° throughout the substrate, preferably within 5°, and more preferably within 3°.

[0051]. The invention also provides a method for the fabrication of flexible and long, single grained semiconductors epitaxially deposited on tapes, and articles formed thereof. As used herein, the phrase "single grain" is defined herein to mean that the semiconductor formed is crystallographically like a bulk single crystal.

[0052].

Table 1 shows some semiconductors and their physical properties such as Si, GaAs, SiC and cubic boron nitride (cBN). Of particular interest are unconventional semiconductors such as diamond.

[0053]. **TABLE I**

Properties	**Diamond**	**Si**	**GaAs**	**SiC**	**cBN**
Lattice constant (Ang)	3.567	5.431	5.653	4.359	3.615
Density (g/cm^3)	3.52	2.42	5.32	3.16	3.48
Thermal conductivity (W/cm-K)	20-150_{max}	1.5	0.5	4.9	13
Dielectric constant	5.68	11.7	10.9	9.7	7.1
Refractive index	2.41	3.44	3.75	2.48	2.12
Bandgap (eV)	5.47	1.11	1.43	2.23	6.6-8.0
Mobility ($cm^2/V.s$) Electrical Hole	1800 1600	1350 480	8600 400	1000 70	1500 450
Saturation Velocity (10^7 cm/s)	2.7	1.0	2.0	2.7	
Breakdown Field (10^7 V/cm)	100	3	4	30	

[0054]. Ir or an Ir alloy can be used as a buffer layer on a substrate, or can serve as the substrate itself. It is critical to the invention that a single-crystal or biaxially textured semiconductor layer is above and in contact with a layer of single-crystal or biaxially textured Ir or Ir Alloy. Suitable Ir alloys include $Ir_{1-x}M_x$ wherein M comprises at least one element selected from the group consisting of Ta, Ti, Cu, Pt, Pd, Ru, Rh, Os, Au, W, and Ag. Fig. 1 shows one embodiment of the invention where a substrate supports a layer of single-crystal or biaxially textured Ir or Ir Alloy, upon which is deposited a semiconductor such as diamond.

[0055]. Suitable substrates can have biaxially textured, substantially biaxially textured, single-grain or untextured surfaces. The substrate can be any suitable material that can support a biaxially textured buffer layer of Ir or its alloy. Suitable substrate materials include, but are not limited to stainless steel, Cu, Ni, Fe, Al, Ag, and alloys of any of the foregoing. Suitable alloying elements include, but are not limited to W, Cr, V, and Mn. Suitable substrate alloys include, but are not limited to Ni-W, Ni-Cr, Ni-Cr-W, Ni-Cr-V, Ni-V, and Ni-Mn. Suitable oxide substrates include, but are not limited to, MgO, $SrTiO_3$, and $REAlO_3$, where RE comprises at least one rare-earth element, namely Y, La, Ce, Pr, , Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho Er, Tm, Yb, and Lu. Substrate/Ir laminates can be prepared by any suitable method, including, but not limited to RABiTS, ion-beam assisted deposition (IBAD), and inclined-substrate deposition (ISD).

[0056]. One or more buffer layers can be deposited on the substrate, to form a buffer system between the substrate and the Ir layer. A buffer system generally comprises the layers between the substrate and the semiconductor layer. Buffer systems in accordance with the present invention can comprise any known architecture, and can be deposited by any known means, as long as there is a layer of biaxially textured Ir present above the buffer system. Some examples of suitable deposition methods include, but are not limited to: physical vapor deposition (PVD) which includes pulsed laser deposition (PLD), electron beam evaporation, sputtering (reactive, rf, dc, for example), etc.; chemical vapor deposition (CVD) which includes metal-organic CVD (MOCVD), sol-gel deposition, metal-organic deposition, spray pyrolysis, plasma spray, etc.; and plating methods such as elctrodeposition and electroless deposition. Fig 2 shows biaxially textured buffer system between the substrate and the Ir.

[0057]. One or more buffer layers can be deposited on the substrate, to form a buffer system between the semiconductor and the Ir layer as well as a buffer between the substrate and the Ir layer. A buffer system generally comprises the layers between the substrate and the semiconductor layer. Buffer systems in accordance with the present invention can comprise any known architecture, and can be deposited by any known means, as long as there is a layer of biaxially textured Ir present above the buffer

system. Some examples of suitable deposition methods include, but are not limited to: physical vapor deposition (PVD) which includes pulsed laser deposition (PLD), electron beam evaporation, sputtering (reactive, rf, dc, for example), etc.; chemical vapor deposition (CVD) which includes metal-organic CVD (MOCVD), sol-gel deposition, metal-organic deposition, spray pyrolysis, plasma spray, etc.; and plating methods such as elctrodeposition and electroless deposition. Fig 3 shows two biaxially textured buffer systems – one between the substrate the Ir, and one between the Ir and the semiconductor.

[0058]. One or more buffer layers can also be deposited on the substrate, to form a buffer system between the Ir layer and the semiconductor. A buffer system generally comprises the layers between the substrate and the semiconductor layer. Buffer systems in accordance with the present invention can comprise any known architecture, and can be deposited by any known means, as long as there is a layer of biaxially textured Ir present above the buffer system. Some examples of suitable deposition methods include, but are not limited to: physical vapor deposition (PVD) which includes pulsed laser deposition (PLD), electron beam evaporation, sputtering (reactive, rf, dc, for example), etc.; chemical vapor deposition (CVD) which includes metal-organic CVD (MOCVD), sol-gel deposition, metal-organic deposition, spray pyrolysis, plasma spray, etc.; and plating methods such as elctrodeposition and electroless deposition. Fig 4 shows one biaxially textured buffer system between the Ir layer and the semiconductor.

[0059]. Fig. 5 shows a substrate of single-grain or biaxially textured Ir or Ir Alloy, upon which is deposited a semiconductor such as diamond. One or more buffer layers can also be deposited on the substrate, to form a buffer system between the semiconductor and the Ir-based single-grain substrate. A buffer system generally comprises the layers between the substrate and the semiconductor layer. Buffer systems in accordance with the present invention can comprise any known architecture, and can be deposited by any known means, as long as there is a layer of biaxially textured Ir present above the buffer system. Some examples of suitable deposition methods include, but are not limited to: physical vapor deposition (PVD) which includes pulsed laser deposition (PLD), electron beam evaporation, sputtering (reactive, rf, dc,

for example), etc.; chemical vapor deposition (CVD) which includes metal-organic CVD (MOCVD), sol-gel deposition, metal-organic deposition, spray pyrolysis, plasma spray, etc.; and plating methods such as elctrodeposition and electroless deposition. Fig 6 shows one biaxially textured buffer system between the Ir substrate and the semiconductor.

[0060]. While there has been shown and described what are at present considered the preferred embodiments of the invention, it will be obvious to those skilled in the art that various changes and modifications can be prepared therein without departing from the scope of the inventions defined by the appended claims.